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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/075,181	02/13/2002	Shane Clifford	303.759US1	7264

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EXAMINER	
YIGDALL, MICHAEL J	
ART UNIT	**PAPER NUMBER**
2192	

MAIL DATE	DELIVERY MODE
07/18/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/075,181	CLIFFORD, SHANE	
	Examiner	Art Unit	
	Michael J. Yigdall	2192	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 May 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *52-56* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *52-56* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on May 7, 2007 has been entered. Claims 52-56 are now pending.

Response to Amendment

2. The rejections of the claims under 35 U.S.C. 103(a) set forth in the previous Office action have been withdrawn in view of Applicant's amendment canceling those claims.

Response to Arguments

3. Applicant's arguments have been considered but are moot in view of the new ground(s) of rejection set forth below. Applicant's amendment necessitated the new ground(s) of rejection.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 52-56 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kalaoja et al., "Feature Modelling of Component-Based Embedded Software" (now made of record,

"Kalaoja") in view of U.S. Patent No. 6,591,152 to Takano (art of record, "Takano") and in view of Choi et al., "Development of Software for the Hard Real-time Controller using Feature-Oriented Reuse Method and CASE Tools" (now made of record, "Choi").

With respect to claim 52 (new), Kalaoja teaches a computerized method comprising:

presenting a group of predefined features in a feature diagram of a user interface, each feature having a corresponding feature model (see, for example, page 450, Figure 5 and first column, fourth and fifth paragraphs, which shows presenting a group of predefined features in a feature diagram of a user interface, and page 449, Figure 4, which shows the corresponding feature model);

Kalaoja does not expressly disclose that the predefined features are predefined semiconductor element features.

However, in an analogous art, Takano teaches modeling and generating computer executable code for a control system that includes controlled elements (see, for example, the abstract). In one example, the controlled elements are semiconductor elements for semiconductor fabrication equipment (see, for example, column 8, lines 2-23).

Furthermore, Kalaoja teaches applying the method to embedded software systems, such as those for computer-controlled industrial equipment and machine automation systems, so as to provide mass customization and reuse for such systems (see, for example, page 444, first column, "Abstract" and "Introduction," first paragraph).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to apply the method of Kalaoja to embedded software systems for semiconductor fabrication equipment, as Takano teaches, such that the predefined features are

predefined semiconductor element features, so as to provide mass customization and reuse for such systems, as Kalaoja suggests.

Kalaoja in view of Takano further teaches:

receiving, at the user interface, a selection of one or more features in the feature diagram to be included in or excluded from a semiconductor element (see, for example, Kalaoja, page 450, first column, last paragraph, which shows receiving a selection of one or more features to include in or exclude from the system).

Kalaoja in view of Takano further teaches generating, as a function of the one of more features, computer executable code, which when executed, causes semiconductor fabrication equipment to fabricate a semiconductor element including the selection (see, for example, Kalaoja, page 445, second column, "Software Production," which shows generating computer executable code based on the selection of one or more features, and see, for example, Takano, column 8, lines 2-23, which shows that when executed, the code causes semiconductor fabrication equipment to fabricate a semiconductor element). In terms of an intermediate statechart, however, Kalaoja and Takano do not expressly disclose:

manipulating a statechart as a function of the one or more features to provide a revised statechart; and

generating, as a function of the revised statechart, computer executable code, which when executed, causes semiconductor fabrication equipment to fabricate a semiconductor element including the selection.

Nonetheless, in an analogous art, Choi teaches generating code for a control system (see, for example, page 131, first column, first complete paragraph), wherein a statechart is derived

from a feature model (see, for example, page 129, Fig. 4, which shows a feature model for the control system, page 130, Fig. 5, which shows a statechart for the control system, and page 131, Fig. 6, which shows that the statechart is based on the feature model). Choi teaches that a statechart made from a feature model expresses the whole domain represented in the feature model (see, for example, page 131, first column, top paragraph).

Furthermore, Takano teaches that the computer executable code is a function of sequence data tables that are presented as flowcharts, timing charts or sequence tables (see, for example, column 8, lines 36-43 and 47-55).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to implement the method of Kalaoja and Takano such that a statechart is manipulated as a function of the one or more features to provide a revised statechart, as Choi suggests, and the computer executable code is generated as a function of the revised statechart, as Takano suggests.

With respect to claim 53 (new), the rejection of claim 52 is incorporated, and Kalaoja in view of Takano and Choi further teaches that a first predefined feature of the group of predefined features includes a feature model requiring inclusion of a second predefined feature, and wherein selection of the first predefined feature causes the second predefined feature to be included in the revised statechart (see, for example, Kalaoja, page 447, first column, first paragraph, which shows an "AND-node" that requires inclusion of a second predefined feature when a first predefined feature is selected).

With respect to claim 54 (new), the rejection of claim 52 is incorporated, and Kalaoja in view of Takano and Choi further teaches that a first predefined feature of the group of predefined features excludes inclusion of a second predefined feature, and wherein selection of the first predefined feature prevents the second predefined feature from being included in the revised statechart (see, for example, Kalaoja, page 447, first column, first paragraph, which shows an "XOR-node" that prevents inclusion of a second predefined feature when a first predefined feature is selected).

With respect to claim 55 (new), the rejection of claim 52 is incorporated, and Kalaoja in view of Takano and Choi further teaches that one or more predefined features of the group of predefined features are designated as default features in their respective feature models, and wherein manipulation of the statechart as a function of the one or more features will cause the default features to be included in the revised statechart unless the default features are selected to be excluded (see, for example, Kalaoja, page 449, first column, last paragraph, which shows designating the default inclusion of one or more features).

With respect to claim 56 (new), the rejection of claim 52 is incorporated, and Kalaoja in view of Takano and Choi further teaches:

deploying the computer executable code to a controller coupled to the semiconductor fabrication equipment (see, for example, Takano, column 18, lines 7-13, which shows deploying the computer executable code to the semiconductor fabrication equipment); and

issuing a command to start execution of the computer executable code within the controller (see, for example, Takano, column 8, lines 60-65, which shows issuing a start mode to start operation of the computer executable code).

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to Applicant's disclosure (see the attached Notice of References Cited).

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael J. Yigdall whose telephone number is (571) 272-3707. The examiner can normally be reached on Monday through Friday from 7:30am to 4:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tuan Q. Dam can be reached on (571) 272-3695. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Michael J. Yigdall
Examiner
Art Unit 2192

mjy

Michael Yigdall